

**Amendments to the Drawings:**

The attached sheets of drawing includes changes to Figures 1-2 and 6. These sheets, which includes Figures 1-2 and 6, replace the original sheets including Figures 1-2 and 6.

Attachment: Replacement Sheet  
Annotated Sheets Showing Changes

**REMARKS/ARGUMENTS**

Claims 1, 7 and 17 are amended by this response. Claims 11-16 are canceled by this response. Therefore, claims 1-10 and 17-19 remain pending.

In the latest office action, the Examiner objected to various portions of the specification and drawings. Accordingly, the specification and drawings have now been amended to remove these objections. Specifically, Figure 1 and the specification have now been amended to delete reference no. "103". Figure 1 has also been amended to correct reference no. "117" to "111", and to add reference nos. "107", "109", and "121" in the appropriate places. Figure 2 and the specification have been amended to delete reference no. "203". Figure 6 has been amended to change the position of reference no. "601", and to add reference no. "603". Applicant has filed replacement sheets for the above-referenced amended Figures. Other portions of the specification have been amended in the manner requested by the Examiner, or to correct errors of typographical nature. No new matter has been added to the application by virtue of these amendments.

In the latest office action, the Examiner requested confirmation of an oral election previously made. Applicants hereby confirm election of Group I claims 1-10 and 17-19, without traverse. Accordingly, the non-elected Group II claims 11-16 are hereby canceled without prejudice to filing divisional applications directed thereto.

The Examiner also indicated certain informalities in claims 1, 7, and 17. These claims have now been amended to address the Examiner's objections.

Claims 1 stands rejected as indefinite under 35 U.S.C. §112, ¶2. Claim 1 has now been amended to provide antecedent basis for the claim terms.

All of the pending claims stand rejected either as anticipated by U.S. patent no. 6,593,185 to Tsai et al. ("the Tsai Patent"), or obvious in light of the Tsai Patent taken in combination with other references. These claim rejections are overcome as follows.

Embodiments in accordance with the present invention relate to methods for forming capacitor structures in semiconductor devices. Particular embodiments of methods in accordance with the present invention fabricate such capacitor structures from arrays of metal structures:

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the method deposits a dielectric layer 301 overlying the surface of the metal via structures. A photoresist material 303 is formed overlying the surface of the dielectric layer, which serves as a hard mask. The photoresist material is exposed and patterned. (¶[0024])

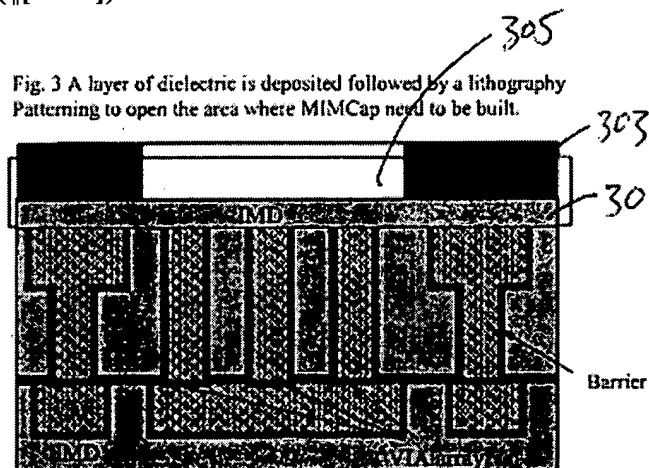


Fig. 3 A layer of dielectric is deposited followed by a lithography Patterning to open the area where MIMCap need to be built.

A selective etching process exposes 401 the barrier layer overlying each of the metal structures, as shown in Figure 4. An opening 403 forms within the capacitor region, excluding the metal structures. (¶[0024])

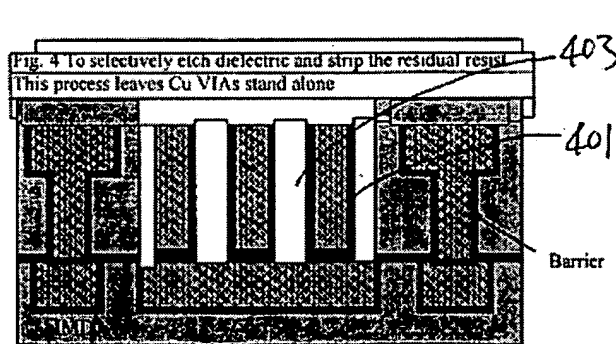
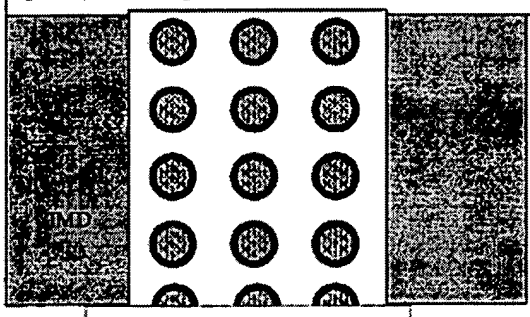


Fig. 4 To selectively etch dielectric and strip the residual resist This process leaves Cu VIAs stand alone

Fig. 5 Top-view of Fig. 4.



Each of the metal structures is substantially parallel to each other in height and is also provided in an array spatial configuration. (Emphasis added; ¶[0024])

As shown in Figure 6 of the instant application, fabrication of the capacitor structure is completed by forming metal within the opening between the arrayed metal structures.

Pending independent claims 1 and 17 have now been amended to recite methods involving formation of an array:

1. A method for manufacturing integrated circuit devices including capacitor structures, the method comprising:  
 . . . patterning a region to expose each of the metal structures to expose the barrier layer overlying each of the metal structures, thereby forming an array;

forming a capacitor insulating layer overlying the array; and  
forming a second metal layer overlying the capacitor insulating layer . . . .

\* \* \*

17. A method for manufacturing integrated circuit devices including capacitor structures, the method comprising:

. . . patterning the capacitor region to expose the barrier layer on each of the metal structures to form an opening within the capacitor region excluding the plurality of metal structures and barrier layer, the plurality of metal structures and barrier layer forming a first electrode array structure of a capacitor;

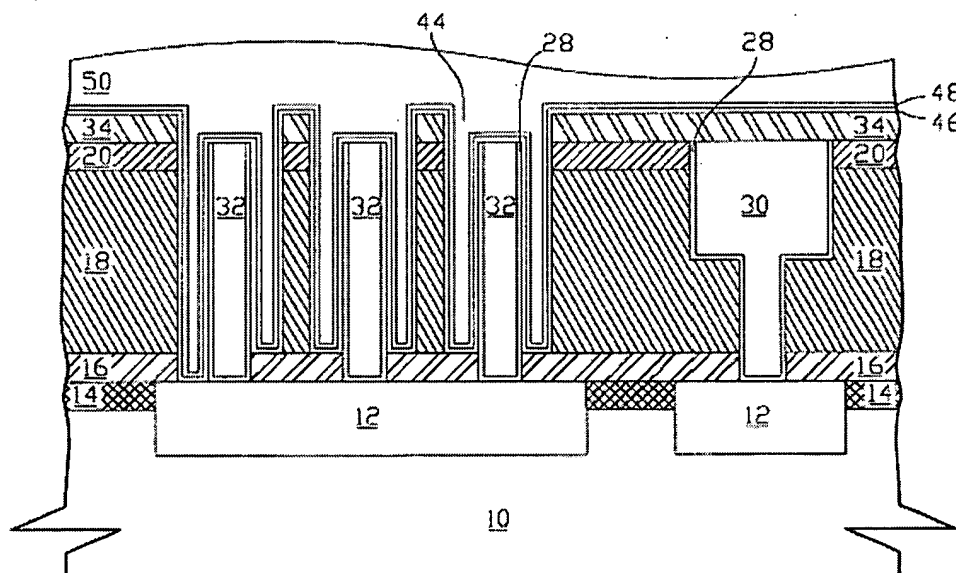
forming an insulating layer overlying each of the exposed barrier layer structures to form a capacitor dielectric for the capacitor;

filling the opening within the capacitor region using a second metal layer overlying the capacitor insulating layer to form a second electrode structure of the capacitor . . . .

Certain of the pending claims stand rejected as anticipated, and not merely obvious, based upon the Tsai Patent. As a threshold matter, the Examiner is reminded:

[t]he distinction between rejections based on 35 U.S.C. 102 and those based on 35 U.S.C. 103 should be kept in mind. Under the former, the claim is anticipated by the reference. No question of obviousness is present. In other words, for anticipation under 35 U.S.C. 102, the reference must teach every aspect of the claimed invention either explicitly or impliedly. Any feature not directly taught must be inherently present. (Emphasis added; MPEP 706.02)

Here, the Tsai Patent fails to teach fabrication of a capacitor structure from a metal array structure. Figure 7 of the Tsai Patent is reproduced below:



As shown in this Figure 7, the capacitor of the Tsai Patent is not formed from an array of metal structures. Rather, metal (50) is formed within an inverse U-type opening (44), defined by the stack comprising first dielectric material (18), first hard mask layer (20), and cap layer (34). None of the components of this stack of material are metals, and thus the Tsai Patent cannot be understood to teach or even suggest formation of a capacitor structure from a metal array.

Because the Tsai Patent relied upon by the Examiner fails to teach every element of the pending claims, explicitly or even impliedly, it is respectfully asserted that the claims cannot be considered anticipated by that reference. Continued rejection of the claims as anticipated is improper, and the claim rejections should be withdrawn.

Other pending claims have been rejected as obvious based upon the Tsai Patent in combination with other references. The Examiner is further reminded that in order to establish a prima facie case of obviousness, the combined prior art references must teach or suggest all of the claim limitations. (MPEP 2143).

As discussed in detail above, the Tsai Patent fails to teach or even suggest forming a capacitor from a metal array structure. None of the other references relied upon by the Examiner supply this absent teaching.

For example, the Examiner has combined the Tsai Patent with U.S. patent no. 6,638,830 to Tsai et al. ("the second Tsai Patent"). However, the second Tsai Patent describes forming a capacitor from a metal structure having a comb type pattern. (See Col. 3, lines 58-65 and Figures 8, 9, and 10). There is no teaching or suggestion in the second Tsai Patent to utilize an array structure as recited in the pending claims.

Similarly, the Examiner has combined the Tsai Patent with U.S. patent no. 6,451,667 to Ning ("the Ning Patent"). However, the Ning Patent also describes forming a capacitor from a metal having a comb type structure. (See Col. 6, lines 1-8 and Figures 9 and 11). There is again no teaching or suggestion in the second Tsai Patent to utilize an array metal structure as recited in the pending claims.

The Examiner has also combined the Tsai Patent with the excerpt from Wolf et al., "Dry Etching for VLSI Fabrication," Silicon Processing for the VLSI Era-Vol 1 Process Technology

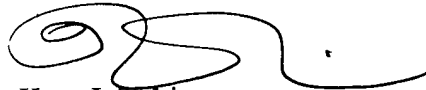
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("the Wolf excerpt"). However, this reference contains no teaching or even suggestion to form a capacitor from a metal array in the claimed manner.

Because the references relied upon by the Examiner, even when combined, fail to teach or suggest every element of the pending claims, it is respectfully asserted that the claims cannot be considered obvious in light of those references. Continued rejection of the claims as obvious is improper, and the claim rejections should be withdrawn.

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested. If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,

A handwritten signature in black ink, appearing to be 'Kent J. Tobin', with a stylized, flowing script.

Kent J. Tobin  
Reg. No. 39,496

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Attachments

RTO:KJT

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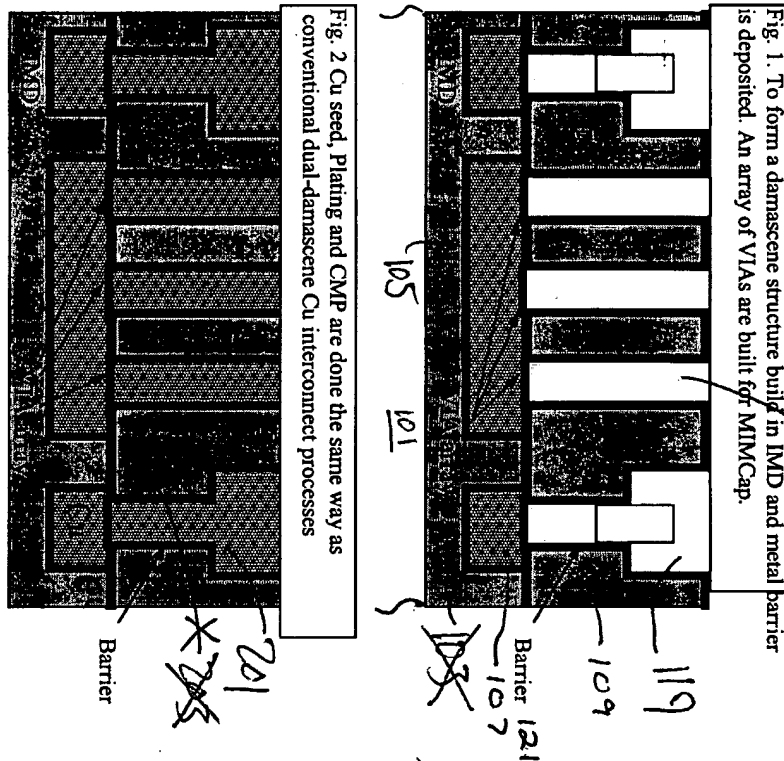


Fig. 3 A layer of dielectric is deposited followed by a lithography patterning to open the area where MIMCap need to be built.

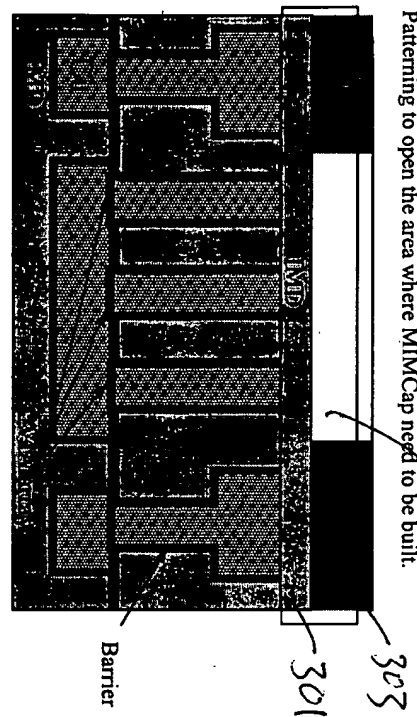


Fig. 4 To selectively etch dielectric and strip the residual resist. This process leaves Cu VIAs stand alone

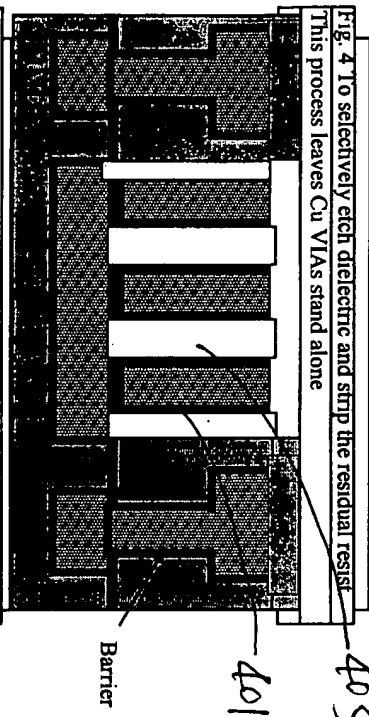
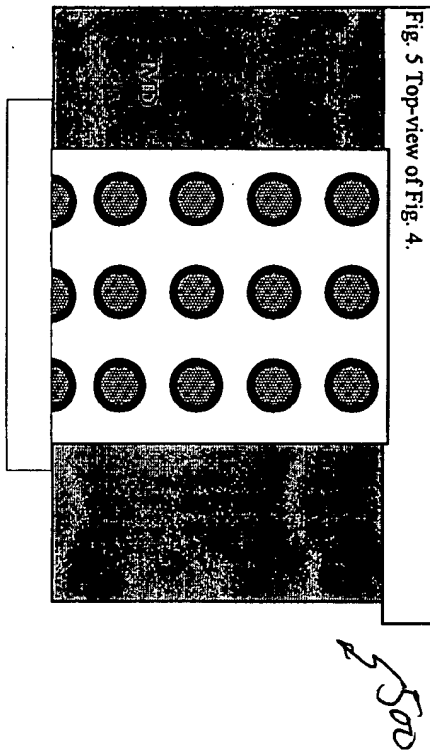


Fig. 5 Top-view of Fig. 4.

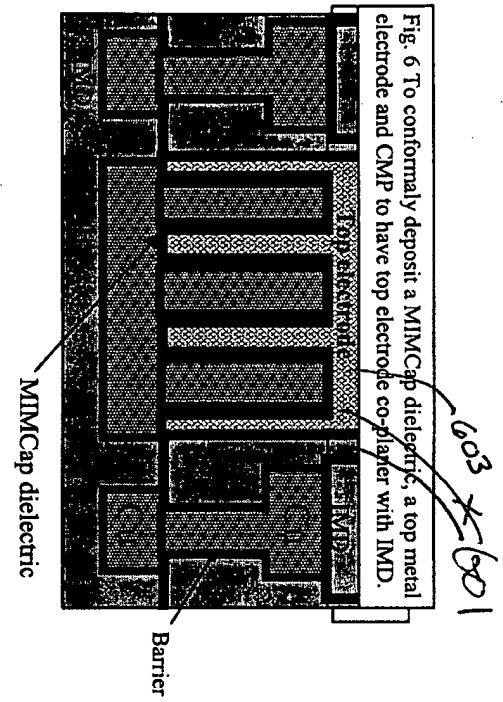


Attorney Docket No.: 021653-001500US

**Title:** Method and Structure of Manufacturing High Capacitance Metal on Insulator Capacitors in Copper

Applicant: Xian Jie Ning

Annotated Drawing Sheet 3 of 3



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